at least a second level of at least four electrically conductive parallel lines extending in the first direction and lying in a second plane above the first plane,

each of the second level lines being disposed over a respective one of the first level lines, such that the lines of the first and second levels are arranged in a series of at least four coplanar line pairs, each line pair comprising one of the first level lines and a respective one of the second level lines;

a dielectric layer disposed between the first and second levels of conductive lines;

D1 cont'd

a plurality of vias arranged in a plurality of groups, each group corresponding uniquely to one of the coplanar line pairs and including at least two vias connecting the first level line and the second level line of the corresponding line pair, thereby forming an array of at least four parallel capacitor plates; and

electrically opposing nodes forming the terminals of the capacitor, the array of parallel capacitor plates electrically connected to the opposing nodes in an alternating manner so that the plates have alternating electrical polarities.

Please add the following new claims:

SUB E1

D2

-- 13. A capacitor comprising:

a first level of at least four electrically conductive parallel lines extending in a first direction above a substrate;

at least a second level of at least four electrically conductive parallel lines

extending in the first direction and lying above the first level,

each of the second level lines being disposed over a corresponding one of the first level lines, such that the lines of the first and second levels are arranged in a series of at least four line pairs, each line pair comprising one of the first level lines and the corresponding one of the second level lines disposed thereover;

a dielectric layer disposed between the first and second levels of conductive lines;

a plurality of groups of vias, each group corresponding to one of the line pairs and including a plurality of vias directly connecting the first level line and the second level line of the corresponding line pair, thereby forming an array of at least four parallel capacitor plates; and

electrically opposing nodes forming the terminals of the capacitor, the array of parallel capacitor plates electrically connected to the opposing nodes in an alternating manner so that the plates have alternating electrical polarities.

14. The capacitor of claim 13, further comprising:

at least a third level of electrically conductive parallel lines extending in the first direction and lying above the first and second levels such that each of the third level lines is disposed over a corresponding one of said line pairs; and

a second dielectric layer disposed between the second and third levels of conductive lines,

wherein the third level of lines vertically extends the array of at least four parallel capacitor plates.

15. The capacitor of claim 13, wherein the vias in each group are identically spaced apart.

16. The capacitor of claim 13, wherein each group includes four vias.

17. The capacitor of claim 13, wherein the each group includes:

a first via directly connecting the first level line and the second level line of the corresponding line pair at respective first ends of the first and second level lines; and

a second via directly connecting the first level line and the second level line of the corresponding line pair at respective second ends of the first and second level lines, wherein the second ends are opposite the first ends along the first direction.

18. A capacitor comprising:

a first level of at least four electrically conductive parallel lines extending in a first direction;

at least a second level of at least four electrically conductive parallel lines extending in the first direction and lying above the first level,

each of the second level lines being disposed over a corresponding one of the first level lines, such that the lines of the first and second levels are arranged in a

series of at least four line pairs, each line pair comprising one of the first level lines and the corresponding one of the second level lines disposed thereover;

SUB E1

a dielectric layer disposed between the first and second levels of conductive lines;

a plurality of groups of vias, each group including a plurality of vias extending directly between the first level line and the second level line of a line pair, thereby forming an array of at least four parallel capacitor plates; and

electrically opposing nodes forming the terminals of the capacitor, the array of parallel capacitor plates electrically connected to the opposing nodes in an alternating manner so that the plates have alternating electrical polarities.

19. The capacitor of claim 18, further comprising:

D2

at least a third level of electrically conductive parallel lines extending in the first direction and lying above the first and second levels such that each of the third level lines is disposed over a corresponding one of said line pairs; and

a second dielectric layer disposed between the second and third levels of conductive lines,

wherein the third level of lines vertically extends the array of at least four parallel capacitor plates.

20. The capacitor of claim 17, wherein each group includes four vias. --